

ABSTRACT

A clock conversion apparatus includes a memory that can perform writing and reading independently from each other, a first counter circuit for controlling write addresses, a delay adjustment circuit for adjusting a delay time of a reading start reference signal from a writing start reference signal, and a second counter circuit for controlling read addresses from the reading start reference signal, wherein data corresponding to a horizontal sync period are written in the memory over plural times to reduce the capacity of the memory, and a writing start position and a reading start position are delay-adjusted.